IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please AMEND claims 1, 3, 13, 15, 21, 22 and 25 and CANCEL claims 4 and 16, without prejudice or disclaimer, in accordance with the following:

1. (Currently Amended) An apparatus generating a clock signal, the apparatus comprising:

a voltage controlled oscillator which generates a clock signal of a frequency that varies with a control voltage signal;

a phase compensator which receives an input signal and the clock signal, detects a phase difference between the input signal and the clock signal, and generates a first control voltage corresponding to the phase difference;

a frequency compensator which receives the input signal and the clock signal, detects a frequency difference between the input signal and the clock signal, and generates a second control voltage corresponding to the frequency difference; and

an adder which sums the first control voltage and the second control voltage and generates the control voltage signal, wherein the frequency compensator comprises a booster which boosts a high-frequency component of the input signal.

2. (Original) The apparatus of claim 1, wherein the input signal is a radio frequency (RF) signal read from data recorded onto an optical disk.

3. (Currently Amended) The apparatus of claim 1, wherein the phase compensator comprises:

a phase detector which receives ~~an~~the input signal and the clock signal and detects a phase difference between the input signal and the clock signal; and

a loop filter which filters an output of the phase detector and outputs ~~a~~the first control voltage corresponding to the phase difference.

4. (Cancelled)

5. (Original) The apparatus of claim 1, wherein the frequency compensator comprises a binarizer which converts the input signal into a digital signal.

6. (Original) The apparatus of claim 1, wherein the frequency compensator further comprises:

a first maximum period detector which counts the number of clock signals within each section where the input signal is positive (+) and outputs a first maximum period for a predetermined amount of time;

a second maximum period detector which counts the number of clock signals within each section where the input signal is negative (-) and outputs a second maximum period for the predetermined amount of time;

a maximum period detector which receives the first maximum period and the second maximum period and determines whether the input signal has an error; and

a frequency error generator which compares the output signal of the maximum period detector with a predetermined value and generates a control voltage corresponding to the difference between the output signal and the predetermined value.

7. (Original) The apparatus of claim 6, wherein the predetermined value is a period of 14T of a sync signal of a digital versatile disk (DVD).

8. (Original) The apparatus of claim 6, wherein when the difference between the first maximum period and the second maximum period is less than a predetermined range, the maximum period detector outputs either the first maximum period or the second maximum period or an average value of the first maximum period and the second maximum period.

9. (Original) The apparatus of claim 6, wherein the maximum period detector additionally receives a signal of a period of T, counts the number of clock signals within each section where the signal is positive (+) or negative (-), compares the count value with the first maximum period or the second maximum period, and outputs one of the count values, the first maximum period, or the second maximum period or an average value of the count value and the first maximum period or an average value of the count value and the second maximum period.

10. (Original) A frequency compensation apparatus comprising:

a first maximum period detector which counts a number of clock signals within each section where an input signal is positive (+) and outputs a first maximum period for a predetermined amount of time;

a second maximum period detector which counts the number of clock signals within each section where the input signal is negative (-) and outputs a second maximum period for the predetermined amount of time;

a maximum period detector which receives a first maximum period and a second maximum period and determines whether the input signal has an error; and

a frequency error generator which compares an output signal of the maximum period detector with a predetermined value and generates a control voltage corresponding to a difference between the output signal and the predetermined value.

11. (Original) The frequency compensation apparatus of claim 10, wherein when a difference between the first maximum period and the second maximum period is less than a predetermined range, the maximum period detector outputs either the first maximum period or the second maximum period or an average value of the first maximum period and the second maximum period.

12. (Original) The frequency compensation apparatus of claim 10, wherein the maximum period detector additionally receives a signal of a period of T, counts the number of clock signals within each section where the signal is positive (+) or negative (-), compares a count value with the first maximum period or the second maximum period, and outputs one of the count value, the first maximum period, or the second maximum period or an average value of the count value and the first maximum period or an average value of the count value and the second maximum period.

13. (Currently Amended) A method of generating a clock signal, the method comprising:

generating a first clock signal of a frequency that varies with a control voltage signal;

receiving an input signal and the first clock signal, detecting a phase difference between the input signal and the first clock signal, and outputting a first control voltage corresponding to the phase difference;

receiving the input signal and the first clock signal, detecting a frequency difference between the input signal and the first clock signal, and outputting a second control voltage corresponding to the frequency difference; and

controlling the frequency of the first clock signal based on ~~a~~the control voltage signal generated by summing the first control voltage and the second control voltage and generating a second clock signal, wherein the outputting of the second control voltage corresponding to the frequency difference comprises receiving the clock signal and a signal generated by boosting a high-frequency component of the input signal, detecting a frequency difference between the clock signal and the signal, and outputting the second control voltage corresponding to the frequency difference.

14. (Original) The method of claim 13, wherein the input signal is a radio frequency (RF) signal read from data recorded onto an optical disk.

15. (Currently Amended) The method of claim 13, wherein the outputting of the first control voltage corresponding to the phase difference comprises:

receiving ~~an~~the input signal and the first clock signal and detecting ~~a~~the phase difference between the input signal and the first clock signal; and

filtering the output of the phase detector and outputting ~~a~~the first control voltage corresponding to the phase difference.

16. (Cancelled)

17. (Original) The method of claim 13, wherein the outputting of the second control voltage corresponding to the frequency difference comprises:

counting a number of clock signals within each section where the input signal is positive (+) and outputting a first maximum count value for a predetermined amount of time;

counting a number of clock signals within each section where the input signal is negative (-) and outputting a second maximum count value for a predetermined amount of time;

receiving, a first maximum period and a second maximum period and determining whether the input signal has an error; and

comparing an output signal of the maximum period detecting unit with a predetermined value and generating a control voltage corresponding to the difference between the output signal and the predetermined value.

18. (Original) The method of claim 17, wherein the predetermined value is a period of 14T of a sync signal of a digital versatile disk (DVD).

19. (Original) The method of claim 17, wherein when the difference between the first maximum period and the second maximum period is less than a predetermined range, outputting either the first maximum period or the second maximum period or an average value of the first maximum period and the second maximum period.

20. (Original) The method of claim 17, wherein in addition to receiving, a first maximum period and a second maximum period and determining whether the input signal has an error, receiving a signal of a period of T, counting the number of clock signals within each section where the signal is positive (+) or negative (-), comparing the count value with the first maximum period or the second maximum period, and outputting one of the count value, the first maximum period, or the second maximum period or an average value of the count value and the first maximum period or an average value of the count value and the second maximum period if the difference between the count value and the first maximum period or the second maximum period is less than the predetermined value.

21. (Currently Amended) A frequency compensation method comprising:

counting a number of clock signals within each section where an input signal is positive (+) or negative (-) and outputting a maximum positive count value and a maximum negative count value;

comparing the maximum positive count value with the maximum negative count value~~receiving a maximum period~~;

~~receiving a signal of a period of T, counting a number of clock signals within each section where the signal is positive (+) or negative (-), and comparing a count value with the maximum period~~; and

if the difference between the maximum positive count value and the maximum ~~period~~negative count value is below a predetermined value, outputting either the maximum positive count value or the maximum ~~period~~negative count value or an average value of the maximum positive count value and the maximum ~~period~~negative count value.

22. (Currently Amended) A computer readable recording medium having embodied

thereon a computer program for a method of generating a clock signal, wherein the method comprises:

generating a first clock signal of a frequency that varies with a control voltage signal;

receiving an input signal and the first clock signal, detecting a phase difference between the input signal and the first clock signal, and outputting a first control voltage corresponding to the phase difference;

receiving the input signal and the first clock signal, detecting a frequency difference between the input signal and the first clock signal, and outputting a second control voltage corresponding to the frequency difference; and

controlling the frequency of the first clock signal based on ~~a~~the control voltage signal generated by summing the first control voltage and the second control voltage and generating a second clock signal, wherein the outputting of the second control voltage corresponding to the frequency difference comprises receiving the clock signal and a signal generated by boosting a high-frequency component of the input signal, detecting a frequency difference between the clock signal and the signal, and outputting the second control voltage corresponding to the frequency difference.

23. (Original) The computer readable recording medium according to claim 22, wherein the computer program is stored in a magnetic tape, a hard disk, a floppy disk, a flash memory, an optical storage media or a carrier wave.

24. (Original) The computer readable recording medium according to claim 22, wherein the computer program is distributed over a computer system connected via a network, and the computer program is stored and implemented as a computer readable code using a distribution technique.

25. (Currently Amended) A computer readable recording medium having embodied thereon a computer program for a frequency compensation method, wherein the frequency compensation method comprises:

~~receiving a maximum period~~counting a number of clock signals within each section where the signal is positive (+) or negative (-), and outputting a maximum positive count value and a maximum negative count value;

~~receiving a signal of a period of T, counting a number of clock signals within each section where the signal is positive (+) or negative (-), and comparing the count value with the maximum~~

~~period~~comparing the maximum positive count value with the maximum negative count value; and

if the difference between the maximum positive count value and the maximum ~~period~~negative count value is below a predetermined value, outputting either the maximum positive count value or the maximum ~~period~~negative count value or an average value of the maximum positive count value and the maximum ~~period~~negative count value.

26. (Original) The computer readable recording medium according to claim 25, wherein the computer program is stored in a magnetic tape, a hard disk, a floppy disk, a flash memory, an optical storage media or a carrier wave.

27. (Original) The computer readable recording medium according to claim 25, wherein the computer program is distributed over a computer system connected via a network, and the computer program is stored and implemented as a computer readable code using a distribution technique.